

# SPECIFICATION

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## ***CONTACT METHOD FOR THIN SILICON CARBIDE EPITAXIAL LAYER AND SEMICONDUCTOR DEVICES FORMED BY THOSE METHODS***

### **Background of Invention**

#### [0001] *FIELD OF THE INVENTION*

[0002] The present invention relates to methods of making semiconductor devices and in particular to methods of providing ohmic contacts to compound semiconductor layers utilized in semiconductor devices.

#### [0003] *DESCRIPTION OF THE RELATED ART*

[0004] The fabrication and operation of basic transistor devices is well known. New technologies have developed needs for higher speed and power transistors capable of withstanding extreme operating conditions such as high temperatures, current, and radiation. Silicon carbide devices have the potential to fulfill these needs but have yet to achieve commercial success. One obstacle to using silicon carbide in electronic devices is the difficulty in providing electrical contacts to the device.

[0005] Electrical contacts to silicon carbide may be formed by reacting a contact metal with silicon carbide. One such method involves melting an alloy on the surface of silicon carbide. When the alloy melts, it dissolves and reacts with a small portion of the silicon carbide to form a contact. A second method of creating a contact involves laminating the surface of the silicon carbide with a contact metal. When annealed, this metal reacts with the silicon carbide to form an ohmic contact. The first method

results in a contact that is too large for use in miniature devices. Annealing temperatures in the second method would be destructive to insulating layers. Both methods are incompatible with semiconductor devices having thin silicon carbide layers because of problems with metal spiking.

[0006] In order to prevent metal spiking, barrier layers between the contact metal and silicon carbide may be used. In one method a portion of doped silicon carbide is bombarded with ions to produce a heavily doped barrier region to which contact is made. Alternatively, a silicide barrier layer may be formed during annealing. Both of these methods are impractical for forming contacts to thin silicon carbide layers. Ion bombardment is not feasible for thin silicon carbide layers because the highly doped region is likely to extend through the entire layer and into an underlying layer. Similarly, the formation of a silicide barrier layer may electrically short a thin silicon carbide layer to an underlying layer because the reaction can consume the entire thickness of the thin silicon carbide layer and a portion of the underlying layer.

## Summary of Invention

[0007] In embodiments described below, the process overcomes the problems above to enable the creation of microscopic contacts and is thus compatible with modern, miniature devices. Another benefit of the described embodiments is that insulating layers created during the process are preserved because of lower process temperatures. Finally, the embodiments described may be used with thin silicon carbide layers without causing electrical shorts through the layer.

[0008] In one set of embodiments, a process for forming a contact to a compound semiconductor layer can comprise forming a first compound semiconductor layer over a substrate. The first compound semiconductor layer may have a first conductivity type. The process can also comprise forming a second compound semiconductor layer. The second compound semiconductor layer may have a second conductivity type that is opposite the first conductivity type. The process can further comprise forming a third compound semiconductor layer. The third compound semiconductor layer may have the first conductivity type. The process can still further comprise patterning the third compound semiconductor layer to define an opening with a wall. The process can also comprise forming an insulating material along the wall, and

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forming a fourth compound semiconductor layer at least partially within the opening. The fourth compound semiconductor layer may have the second conductivity type and a dopant concentration that is higher than a dopant concentration of the second compound semiconductor layer. The fourth compound semiconductor layer may also be electrically connected to the second compound semiconductor layer and may be insulated from the third compound semiconductor layer.

[0009] In another set of embodiments, a semiconductor device can comprise a first active layer including a first compound semiconductor material and having a first conductivity type. The semiconductor device may also comprise a second active layer including a second compound semiconductor material and having a second conductivity type opposite the first conductivity type. The second active layer can contact the first active layer. The semiconductor device may further comprise a third active layer that includes a third compound semiconductor material having the first conductivity type. The third active layer can contact the second active layer, and a combination of the first, second, and third active layers can be at least part of a transistor. An opening may extend through the third active layer and contact the second active layer. The semiconductor device can still further comprise a fourth compound semiconductor material at least partially within the opening. The fourth compound semiconductor material may have the second conductivity type and a dopant concentration higher than a dopant concentration of the second active layer and may be electrically connected to the second active layer. The semiconductor device can also comprise a first insulating layer at least partially within opening. The first insulating layer may lie between the third active layer and the fourth compound semiconductor layer.

[0010] The foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

## Brief Description of Drawings

[0011] The present invention is illustrated by way of example and not limitation in the accompanying figures.

[0012] FIG. 1 includes an illustration of a cross-sectional view of a portion of a substrate

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after forming first, second, and third active layers.

[0013] FIG. 2 includes an illustration of a cross-sectional view of the substrate of FIG. 1 after patterning the third active layer to define openings.

[0014] FIG. 3 includes an illustration of a cross-sectional view of the substrate of FIG. 2 after forming an insulating layer over the third active layer and within the openings.

[0015] FIG. 4 includes an illustration of a cross-sectional view of the substrate of FIG. 3 after planarizing and etching the insulating layer to expose the second active layer at the bottom of the trenches.

[0016] FIG. 5 includes an illustration of a cross-sectional view of the substrate of FIG. 4 after forming a layer of heavily doped silicon carbide deposited in the trenches.

[0017] FIG. 6 included an illustration of a cross-sectional view of the substrate of FIG. 5 after removing portions of the heavily doped silicon carbide layer lying outside the openings.

[0018] FIG. 7 includes an illustration of a cross-sectional view of the substrate of FIG. 6 after forming metal contacts to the second and third active layers.

[0019] FIG. 8 includes an illustration of a cross-sectional view of the substrate of FIG. 7 after forming an insulating layer over the third active layer and metal contacts.

[0020] FIG. 9 includes an illustration of a cross-sectional view of the substrate of FIG. 8 after removing a portion of the insulating layer to expose surfaces of the metal contacts.

[0021] Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

## Detailed Description

[0022]

Reference is now made in detail to the exemplary embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible,

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the same reference numbers will be used throughout the drawings to refer to the same or like parts (elements).

[0023] Described generally below is a process for fabricating an electrical connection between a metal contact and a thin layer of silicon carbide while reducing the likelihood of spiking of the silicon carbide layer. The contact process is described in the context of fabricating a planar, multi-layered silicon carbide device, but as one skilled in the art may surmise, it may be used for forming connections between any applicable metal and silicon carbide layer.

[0024] FIG. 1 includes an illustration of a portion of a substrate 10. The substrate 10 may include silicon carbide, gallium nitride, aluminum nitride, or other wide bandgap semiconductors. A wide bandgap material will have a bandgap of about 3 eV or greater. Active layers 12, 14, and 16 are sequentially formed over the substrate 10. Each of the active layers 12, 14, and 16 may be formed using conventional epitaxial growing techniques and comprise one or more compound semiconductor materials. A compound semiconductor includes at least two dissimilar elements that form a semiconductor material. In one specific example, at least two dissimilar Group IVA elements such as carbon, silicon, or germanium can be part of the semiconductor material. Silicon carbide (SiC) is an example of a compound semiconductor material having Group IVA elements. In this particular embodiment, layers 12, 14, and 16 can comprise SiC. SiC polytype 4H may be used as well as 6H, 3C, or other similarly reactive polytypes.

[0025] Layer 12 can have a thickness in a range of approximately 2–20 microns, can be n-type doped with nitrogen, phosphorus, or the like, and can have a dopant concentration in a range of approximately 1E15 to 1E18 atoms per cubic centimeter. Layer 14 can have a thickness in a range of approximately 0.1–2.0 microns, can be p-type doped with aluminum, boron, or the like, and have a dopant concentration in a range of approximately 1E15 to 1E17 atoms per cubic centimeters. Layer 16 can have a thickness in a range of approximately 0.5–2.0 microns, can be n-type doped with nitrogen, phosphorus, or the like, and have a dopant concentration in a range of approximately 1E17 to 1E19 per cubic centimeters. Layer 12 may be a collector, layer 14 may be a base, and layer 16 may be an emitter of a transistor.

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[0026] Next, openings 20 can be formed by masking layer 16 with aluminum, nickel, or the like (not shown) and etching layer 16. The openings 20 extend through layer 16 and expose a portion of layer 14. A reactive ion etch (RIE) in an ionized  $\text{CF}_4/\text{O}_2/\text{H}_2$  atmosphere may be used.

[0027] An insulating layer 30, capable of being anisotropically etched, is then deposited on the exposed surfaces of layer 16 and at least partially within the openings 20 as shown in FIG. 3. An insulator such as silicon dioxide, silicon nitride, silicon oxynitride, or the like may be used for insulating layer 30. The insulating layer 30 can serve to passivate the walls of the opening 20 and insulate layer 16 from a subsequently formed material that may be electrically connected to layer 14. Portions of insulating layer 30 may be mechanically or chemically removed to expose layer 16. Then insulating layer 30 is masked and the insulating material in the openings 20 is anisotropically etched to expose a portion of layer 14 as illustrated in FIG 4. A typical anisotropic etch may be a  $\text{CF}_4/\text{O}_2$ -based reactive ion etch.

[0028] As shown in FIG. 5, a heavily doped SiC layer 50 is then sputtered on to layer 14. The layer 50 may be RF sputtered at a power in the range of approximately 100–200 watts using a SiC target. Sputtering may be done at low pressure in the range of approximately 50–200 mTorr, in the presence of a non-reactive gas such as argon. During sputtering, the substrate may be held at a temperature in a range of approximately 800 °C 1100 °C, which is below the melting temperature of the insulating layer 30, which is roughly 1100 °C.

[0029] The desired dopant concentration for the SiC layer 50 is in the range of approximately 1E19–1E20 atoms per cubic centimeter. Dopants can be incorporated by simultaneously co-sputtering, DC sputtering, or by sputtering in the presence of a gas. For example, aluminum may be incorporated by simultaneously co-sputtering, DC sputtering from an aluminum target, or by sputtering in the presence of gaseous trimethyl aluminum ( $\text{Al}(\text{CH}_3)_3$ ). Aluminum may be sputtered with a power in the range of approximately 10–50 watts of DC power. An alternative p-dopant may be boron, which can be added as gaseous diborane ( $\text{B}_2\text{H}_6$ ). Alternatively, the dopants can be alloyed with the silicon carbide target.

[0030] *Portions of SiC layer 50 overlying the third active layer 16 may be mechanically or*

chemically removed to expose portions of layer 16, leaving SiC material 50 at least partially within openings 20, as illustrated in FIG. 6.

[0031] Illustrated in FIG. 7, a metal layer 70 may be deposited on the heavily doped silicon carbide 60. The metal layer 70 may be aluminum or any other metal that can form an ohmic contact to p-doped silicon carbide. A metal layer 72 may be deposited on n-doped silicon carbide layer 16. The metal layer 72 on layer 16 can be nickel or any other metal that can form an ohmic contact to n-doped silicon carbide. The metal layers 70 and 72 can be deposited by any of a number of methods, including DC sputtering, RF sputtering, thermal evaporation, e-beam evaporation and chemical vapor deposition. The metal layers 70 and 72 may be patterned by photolithography and wet or dry chemical etching.

[0032] The metal layers 70 and 72 can be annealed to form an ohmic electrical connection or contact with the underlying silicon carbide. Depending upon the metal, the annealing temperature may be in a range of approximately 600 ° C 1100 ° C, which is below the melting temperature of the insulating layer 30. Due to the thickness of the heavily doped silicon carbide layer 50, the reaction region 74 between the metal contact 70 and the heavily doped silicon carbide 50 that occurs when the metal is annealed should not extend through the thin layer 14. In this particular embodiment, region 74 does not physically contact layer 14.

[0033] Insulating layer 80 can be deposited on layer 16 and metal layers 70 and 72 as shown in FIG. 8. Layer 80 may be an insulator such as silicon dioxide, silicon nitride, silicon oxynitride, or the like. The insulating layer 80 may then be mechanically or chemically removed to expose surfaces of metal layers 70 and 72 as illustrated in FIG. 9. Wire leads (not shown) may be soldered, bonded, or otherwise electrically connected to the metal layer 70 and 72 contacts. For basic transistor operation, an additional wire lead can be attached to layer 12 to form a substantially completed semiconductor device.

[0034] Additional compound semiconductor layers having appropriate contacts and conductivity types may be incorporated to create devices such as thyristors.

[0035] Accordingly, devices produced can exhibit faster performance because the active

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layer 14 can be thin and not exhibit high contact resistance or junction spiking. Further, high temperature anneals are not required at stages where insulating material may be damaged, thus processing is simplified and reduced. Also, as shown in FIG. 9, the device has an exposed surface that is substantially planar, making the semiconductor device easier to integrate and make external connections to than conventional multi-leveled devices. Because of the higher band-gap and chemical stability of silicon carbide, devices described herein may be used in higher power applications and at higher temperature or radiation levels than traditional silicon devices. The increased power handling capability and temperature resistance of silicon carbide devices also allows for the manufacture of smaller devices than with conventional silicon devices.

[0036] Because of these benefits, transistors produced according to the process described herein may operate in any standard transistor application and are particularly suited for wireless communication base amplifiers or high power switching devices where these devices may be smaller and faster than existing devices. In RF applications such as amplification, the devices may handle approximately 120 volts and up to approximately 5 watts per millimeter perimeter at roughly 3 gigahertz. Power switching devices may handle approximately 2000 volts and may have a switching frequency around 1 megahertz. Devices can be scalable so that greater power levels may be utilized.

[0037] In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

[0038] Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms

"comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

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